



# **Stratix II GX Early SSN Estimator User Guide**

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101 Innovation Drive  
San Jose, CA 95134  
[www.altera.com](http://www.altera.com)

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# About this User Guide

**Revision History** The following table shows the revision history for the chapters in this User Guide.

Date/Version	Changes Made	Summary of Changes
August 2007, v1.0	Initial release	—

## How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	<a href="http://www.altera.com/support">www.altera.com/support</a>
Technical training	Website	<a href="http://www.altera.com/training">www.altera.com/training</a>
	Email	<a href="mailto:custrain@altera.com">custrain@altera.com</a>
Product literature	Website	<a href="http://www.altera.com/literature">www.altera.com/literature</a>
Altera literature services	Email	<a href="mailto:literature@altera.com">literature@altera.com</a>
Non-technical support (General) (Software Licensing)	Email	<a href="mailto:nacomp@altera.com">nacomp@altera.com</a>
	Email	<a href="mailto:authorization@altera.com">authorization@altera.com</a>








*Note to table:*

(1) You can also contact your local Altera sales office or sales representative.

## Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
<b>Bold Type with Initial Capital Letters</b>	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: <b>Save As</b> dialog box.
<b>bold type</b>	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: <b>f<sub>MAX</sub></b> , <b>lqdesigns</b> directory, <b>d:</b> drive, <b>chiptrip.gdf</b> file.
<i>Italic Type with Initial Capital Letters</i>	Document titles are shown in italic type with initial capital letters. Example: <i>AN 75: High-Speed Board Design</i> .

Visual Cue	Meaning
<i>Italic type</i>	Internal timing parameters and variables are shown in italic type. Examples: $t_{PIA}$ , $n + 1$ .  Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <file name>, <project name>.pdf file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
“Subheading Title”	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: “Typographic Conventions.”
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input. Active-low signals are denoted by suffix n, e.g., resetn.  Anything that must be typed exactly as it displays is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TRI) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets are used in a list of items when the sequence of the items is not important.
	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
	A warning calls attention to a condition or possible situation that can cause injury to the user.
	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

## Introduction

Printed circuit board (PCB) designers need a rough estimate of the amount of simultaneous switching noise (SSN) seen in their designs during the early design phase, without going through extensive pre/post layout simulations. The Stratix II® GX early SSN estimator provides this critical piece of information.

The early SSN estimator (ESE) is a Microsoft Excel-based spreadsheet tool for calculating the worst-case Quiet Low /Quiet High noise seen at the far end of the victim pin induced by multiple aggressors switching simultaneously. The calculator assumes typical process, voltage, and temperature (PVT) conditions for the Stratix II GX device and the PCB board under development. The spreadsheet requires only basic design specific information such as the I/O standard, current strength, and number of simultaneous switching I/Os. The results obtained through the spreadsheet tool are intended only as an estimate of the worst case noise, and not as a specification. The actual results observed on your board may vary due to differences between your PCB design and the assumed typical design conditions used by the calculator. For designers who intend to get a very accurate noise estimate based on their specific PCB design, Altera® recommends a post-layout simulation approach, taking into account the various parameters (board stackup, via breakout, power delivery network design, trace spacing, and so on) specific to the design.

This user guide explains how to use the early SSN estimator to estimate the far-end noise induced on the victim pin.

## Application of the Tool

As described earlier, the purpose of the tool is to provide a rough estimate on the amount of simultaneous switching noise within the design during the early design phase. This spreadsheet tool is very handy to explore the various “what-if” scenarios to study the impact on the observed noise seen using different drive strengths, various number of simultaneous switching I/Os, different VCCIO voltage standards, and so on.

## Setting up the Early SSN Estimator

The ESE spreadsheet consists of various fields tabs shown in [Figure 1-1](#) are as follows:

- **Calculator:** The calculator tab is the primary tab where you input all the relevant design information to estimate the amount of SSN noise.
- **Data Viewer:** The data viewer tab gives a schematic view of the noise profile of individual IO standards as a function of the number of I/Os. The data viewer tab is independent of the calculator tab. It will only display the noise profile of the I/O standard that is set in the data viewer tab irrespective of the I/O standards that are selected for the various banks in the calculator tab.
- **Release Notes:** This tab contains information regarding the current version of the tool. It also lists the changes from the previous versions of the tool.
- **Signal Integrity Center:** This tab provides a link to information dedicated exclusively to signal integrity on Altera's website ([www.altera.com](http://www.altera.com)).
- **Reset:** This tab is used to clear all the data that was entered into the calculator tab.

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**Figure 1-1. Tabs in the ESE Tool**



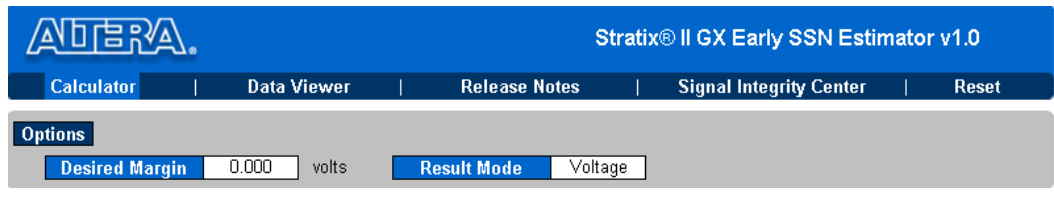
In the calculator tab, there are two kinds of parameters.

- Global parameters
- Parameters Specific to I/O Bank

### Global Parameters

[Figure 1-2](#) shows the global parameters (Desired Margin, Result Mode) listed under the "Options" section in the calculator tab. By default the ESE calculates the far-end noise, assuming a worst-case placement of pins. The worst-case pin placement assumes that aggressor pins are packed as closely as possible to the worst case victim pin.

Figure 1–2. Defining Global Parameters



### *Desired Margin*

The desired margin sets the amount of margin that you wish to allocate for non-SSN related items. This margin is applicable for all the banks that are populated in the calculator tab. By default, the ESE assumes that the entire noise margin is allocated to SSN. This can be entered in either volts or percentage of noise margin, depending on the setting you chose in the Result Mode.

### *Result Mode*

The ESE can report results using two different formats, volts and percentage margin. The default format is to report both noise and margins in volts. When in percentage margin mode, noise is still reported as volts but the margin is expressed as a percentage of the total zero-noise margin. The noise margin is calculated using the following equations:

### *Scenario 1*

#### **Victim net driven Low:**

$$V_{IL \text{ margin } (K)} = \left\{ 1 - \frac{(QLN_{(K)} - QL)}{(VIL_{Max(DC)} - QL)} \right\} * 100 \text{ where}$$

$V_{IL \text{ margin } (K)}$  = Signal Margin Low when K aggressors are switching simultaneously

K = Number of I/Os switching simultaneously

$QLN_{(K)}$  = Quiet Low Noise when K aggressors are switching simultaneously

QL = Quiet Low Voltage (No aggressors switching)

$V_{IL \text{ Max } (DC)}$  = Receiver Maximum DC Input Low Voltage

Scenario 2

Victim Net driven High:

$$V_{IH \text{ margin } (K)} = \left\{ 1 - \frac{(QH - QHN_{(K)})}{(QH - V_{IH \text{ Min}(DC)})} \right\} * 100 \text{ where}$$

$V_{IH \text{ margin } (K)}$  = Signal Margin High when K aggressors are switching simultaneously

K = Number of I/Os switching simultaneously

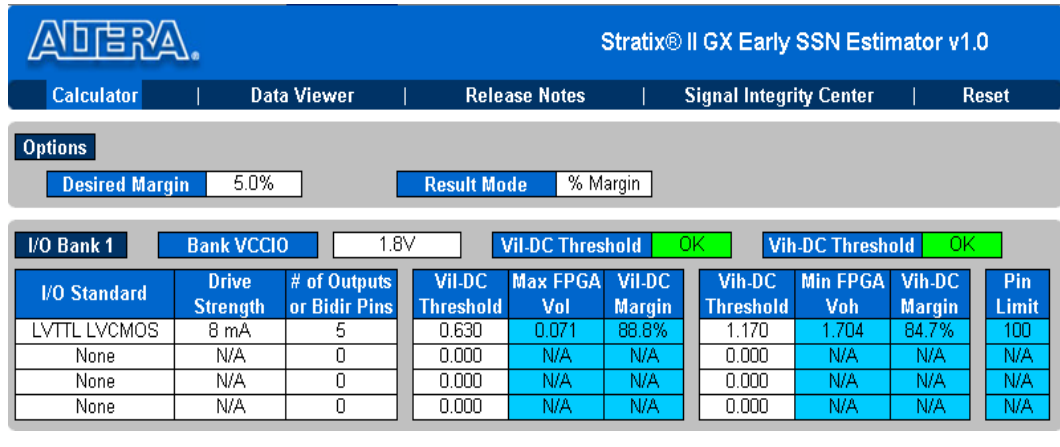
$QHN_{(K)}$  = Quiet High Noise when K aggressors are switching simultaneously

QH = Quiet High Voltage (No aggressors switching)

$V_{IH \text{ Min}(DC)}$  = Receiver Minimum DC Input High Voltage

Figure 1-3 shows the ESE estimator for Bank1 when five I/Os are switching simultaneously using LVTTTL18 8 mA drive strength interface. The example in Figure 1-3 goes through the calculation to arrive at the  $V_{IL}/V_{IH}$  margin that is being reported by the ESE tool.

Figure 1-3.  $V_{IL}/V_{IH}$  Margin Calculation



From the screen above for the victim driven low, the various parameters are as follows:

$$K = 5$$

$$QLN_{(5)} = 0.071 \text{ V}$$

$$QL = 0$$

$$V_{IL \text{ max (DC)}} = 0.630 \text{ V}$$

$$V_{IL \text{ margin (5)}} = \{1 - [(0.071 - 0)/(0.63 - 0)]\} * 100 = 88.73\%$$

Similarly, for the victim driven high, the various parameters are as follows:

$$K = 5$$

$$QHN_{(5)} = 1.704 \text{ V}$$

$$QH = 1.8 \text{ V}$$

$$V_{IH \text{ min (DC)}} = 1.17 \text{ V}$$

$$V_{IH \text{ margin (5)}} = \{1 - [(1.8 - 1.704)/(1.8 - 1.17)]\} * 100 = 84.76\%$$

## Parameters Specific to I/O Bank

Figure 1-4 gives a snapshot of the ESE showing the various parameters for a given bank.

**Bank VCCIO:** Altera I/O banks support only one VCCIO voltage at a time. All I/O standards in the given bank will use this VCCIO. You need to select the Bank VCCIO voltage before selecting the I/O standards for that I/O bank.

**I/O Standard:** The calculator supports mixing up to four different I/O standards in a single bank. If the I/O standard you are interested in is not shown in the drop down box, ensure that the bank VCCIO voltage has been set correctly.

**Drive Strength:** Altera devices support multiple drive strengths depending on the I/O standard. This drop down menu allows you to select valid values.

**Number of Outputs or Bidirectional Pins:** The ESE models simultaneously switching output induced SSN. Switching inputs are not modeled because the ESE has no information on what device is driving an FPGA input. Enter the number of outputs or bidirectional pins that correspond to your selected I/O standard and drive strength.

**$V_{IL(DC)}$ / $V_{IH(DC)}$  Thresholds:** The ESE bases its margin estimates on the input thresholds of the receiving device. By default the  $V_{IL(DC)}$  and  $V_{IH(DC)}$  parameters are automatically populated with their I/O standard specific values when an I/O standard is selected. The values can be manually changed to any threshold values.

Figure 1–4. Parameters Specific to I/O Bank

I/O Standard	Drive Strength	# of Outputs or Bidir Pins	Vil-DC Threshold	Max FPGA Vol	Vil-DC Margin	Vih-DC Threshold	Min FPGA Voh	Vih-DC Margin	Pin Limit
HSTL Class I	8 mA	5	0.800	0.456	0.344	1.000	1.362	0.362	100
HSTL Class II	16 mA	10	0.800	0.497	0.303	1.000	1.317	0.317	100
LVTTTL LVCMOS	4 mA	2	0.630	0.195	0.435	1.170	1.603	0.433	100
LVTTTL LVCMOS	8 mA	2	0.630	0.195	0.435	1.170	1.603	0.433	100

## Interpreting Early SSN Estimator Results

The Stratix II GX ESE reports four types of results for use in guiding your early I/O design: output low/high voltages, input threshold margins, margin okay indicators, and maximum pin limit.

**Max FPGA  $V_{OL}$ :** The maximum voltage output low parameter reports the highest voltage that an FPGA pin can output, when driving a low value, taking into account the SSN induced noise.

**Min FPGA  $V_{OH}$ :** The minimum voltage output high parameter reports the lowest voltage that an FPGA pin can output, when driving a high value, taking into account SSN induced noise.

**$V_{IL}$  Margin/ $V_{IH}$  Margin:** This parameter indicates how much additional noise would be required to violate the  $V_{IL(DC)}$  voltage input low, or  $V_{IH(DC)}$  voltage input high thresholds at the receiver.

**$V_{IL}/V_{IH}$  Threshold Indicator:** The indicators are a quick way to verify if all the I/O standards of a given bank have sufficient margin. If all the checks pass the indicators are green. If any margin is violated the indicators turn red.

**Pin Limit:** The pin limit indicates the maximum number of pins of the corresponding I/O standard that can be used without violating any noise margins, assuming that all other I/O standard pin counts are held constant. If the pin limit column is populated, it indicates there is sufficient margin available and the  $V_{IL}/V_{IH}$  threshold indicators should be green.

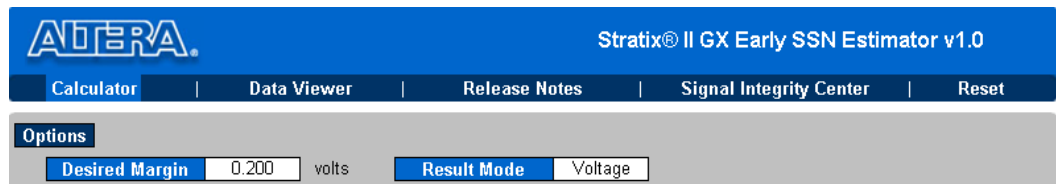
## Tutorial: Mixing SSTL and LVTTTL in a Single Bank

Engineer Bob would like to add a 2.5 V LVTTTL pin to a bank filled with 60 2.5 V SSTL Class II 24 mA drivers. Bob is targeting a voltage margin of 200 mV to account for other non-ssn related items. Use the ESE to determine if Bob might have any problems.

### Step 1: Configure the global parameters

1. Configure the result mode to display results in **Voltage**.
2. Enter a desired margin of **0.2** volts, as shown in [Figure 1–5](#).

Figure 1–5. Global Parameters Configuration



### Step 2: Assign the I/O standards to the corresponding bank

1. Set I/O Bank 1 VCCIO to **2.5 V**.
2. Select **I/O Standard SSTL Class II** in row one.
3. Select a drive strength of **24 mA**.
4. Enter **60** as the number of output pins.
5. Select **I/O standard LVTTTL** in row two.
6. Select a drive strength of **16 mA**.
7. Enter **1** as the number of output pins shown in [Figure 1–6](#).

Figure 1–6. Local Parameters Assignment

I/O Standard	Drive Strength	# of Outputs or Bidir Pins	Vil-DC Threshold	Max FPGA Vol	Vil-DC Margin	Vih-DC Threshold	Min FPGA Voh	Vih-DC Margin	Pin Limit
SSTL Class II	24 mA	60	1.070	0.757	0.313	1.430	1.679	0.249	58
LVTTTL LVCMOS	16 mA	1	0.700	0.478	0.222	1.700	1.891	0.191	0
None	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A
None	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A

### Step 3: Interpret the Results

- The  $V_{IH}$  threshold indicator is red indicating that a margin has been violated.
- The  $V_{IH}$  margin for LVTTTL is 0.191 V (less than 0.2 V that Bob wants for his design). This is highlighted in red to indicate that it is lower than the desired margin.
- The pin limit for SSTL Class II is 58 pins. This means that if the number of outputs for SSTL Class II is reduced to 58, the margin will no longer be violated.
- The pin limit for LVTTTL is 0 pins. This means that no number of LVTTTL pins can be safely combined with 58 SSTL Class II pins under the entered drive strengths for the given desired margin of 0.2 V set by Bob.

## Step 4: Fixing the problem

There are multiple approaches to fix the issue that Bob is observing.

### First Approach:

Reduce the amount of margin that Bob wishes to allocate for non-ssn related items from 200 mV to 175 mV as shown in [Figure 1-7](#).

The pin limit for SSTL Class II I/Os increased from 58 I/Os to 63 I/Os, thereby allowing Bob to implement his SSTL design with 60 I/Os along with 1 LVTTTL output.

**Figure 1-7. First Approach**

I/O Standard	Drive Strength	# of Outputs or Bidir Pins	Vil-DC Threshold	Max FPGA Vol	Vil-DC Margin	Vih-DC Threshold	Min FPGA Voh	Vih-DC Margin	Pin Limit
SSTL Class II	24 mA	60	1.070	0.757	0.313	1.430	1.679	0.249	63
LVTTTL LVCMOS	16 mA	1	0.700	0.478	0.222	1.700	1.891	0.191	1
None	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A
None	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A

### Second Approach:

If timing margin allows, reduce the current drive strength for the SSTL Class II buffers from 24 mA to 20 mA keeping the desired voltage margin at 200 mV for non-ssn related items shown in [Figure 1-8](#).

This decrease in drive strength reduces the SSN noise sufficiently to allow him to implement his design with 60 SSTL I/Os along with 1 LVTTTL I/O with sufficient margin.

Figure 1–8. Second Approach

**Altera** Stratix® II GX Early SSN Estimator v1.0

Calculator | Data Viewer | Release Notes | Signal Integrity Center | Reset

**Options**

Desired Margin: 0.200 volts | Result Mode: Voltage

I/O Bank 1 | Bank VCCIO: 2.5V | Vil-DC Threshold: OK | Vih-DC Threshold: OK

I/O Standard	Drive Strength	# of Outputs or Bidir Pins	Vil-DC Threshold	Max FPGA Vol	Vil-DC Margin	Vih-DC Threshold	Min FPGA Voh	Vih-DC Margin	Pin Limit
SSTL Class II	20 mA	60	1.070	0.748	0.322	1.430	1.707	0.277	83
LVTTTL LVCMOS	16 mA	1	0.700	0.408	0.292	1.700	1.980	0.280	4
None	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A
None	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A

Refer to *AN 472: Stratix II GX SSN Design Guidelines* for additional approaches when designing their boards using Stratix II GX.