



Stratix III Early SSN Estimator User Guide



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About this User Guide

Revision History The following table shows the revision history for the chapters in this user guide.

Date/Version	Changes Made	Summary of Changes
June 2008, v1.0	Initial release	—

How to Contact Altera For the most up-to-date information about Altera products, refer to the following table.








Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Altera literature services	Email	literature@altera.com
Non-technical support (General) (Software Licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com

Note to table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: Save As dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: f_{MAX} , lqdesigns directory, d: drive, chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Document titles are shown in italic type with initial capital letters. Example: <i>AN 75: High-Speed Board Design</i> .

Visual Cue	Meaning
<i>Italic type</i>	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA} , $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <file name>, <project name>.pdf file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
“Subheading Title”	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: “Typographic Conventions.”
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input. Active-low signals are denoted by suffix n, e.g., resetn. Anything that must be typed exactly as it displays is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TRI) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets are used in a list of items when the sequence of the items is not important.
	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
	A warning calls attention to a condition or possible situation that can cause injury to the user.
	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Introduction

Printed circuit board (PCB) designers need to estimate the simultaneous switching noise (SSN) in their designs during the early design phase, without going through extensive pre and post layout simulations. The Stratix® III early SSN estimator provides this critical piece of information.

The early SSN estimator (ESE) is a Microsoft Excel-based spreadsheet tool for calculating the worst-case quiet low/quiet high noise seen at the far end of the victim pin induced by multiple aggressors switching simultaneously. The calculator assumes typical process, voltage, and temperature (PVT) conditions for the Stratix III device and the PCB board under development. The spreadsheet requires only basic design-specific information such as the I/O standard, current strength, slew rate, and number of simultaneous switching I/Os.

The results obtained through the spreadsheet tool are intended only as an estimate of the worst case noise and not as a specification. The actual results observed on your board may vary due to differences between your PCB design and the assumed typical design conditions used by the calculator. For designers who intend to get a very accurate noise estimate based on their specific PCB design, Altera recommends a post-layout simulation approach, taking into account the various parameters such as board stackup, via breakout, power delivery network design, and trace spacing specific to the design.

This user guide explains how to use the early SSN estimator to estimate the far-end noise induced on the victim pin.

Application of the Tool

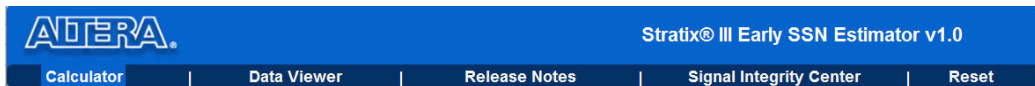
The purpose of the tool is to provide a rough estimate on the amount of SSN within the design during the early design phase. This spreadsheet tool is very useful to explore the various “what-if” scenarios to study the impact on the observed noise seen using different drive strengths, various number of simultaneous switching I/Os, different VCCIO voltage standards, and various I/O settings.

Setting up the Early SSN Estimator

The ESE spreadsheet consists of various field tabs shown in [Figure 1-1](#) and are as follows:

- **Calculator:** The **Calculator** tab is the primary tab where you input the relevant design information to estimate the amount of SSN noise.
- **Data Viewer:** The **Data Viewer** tab gives a schematic view of the noise profile of individual IO standards as a function of the number of I/Os. The **Data Viewer** tab is independent of the **Calculator** tab. It only displays the noise profile of the I/O standard that is set in the **Data Viewer** tab irrespective of the I/O standards that are selected for the various banks in the **Calculator** tab.
- **Release Notes:** The **Release Notes** tab contains information regarding the current version of the tool. It also lists the changes from the previous versions of the tool.
- **Signal Integrity Center:** The **Signal Integrity Center** tab provides a link to information dedicated exclusively to signal integrity on Altera's website (www.altera.com).
- **Reset:** The **Reset** tab is used to clear all the data that is entered into the **Calculator** tab.

Figure 1-1. Tabs in the ESE Tool



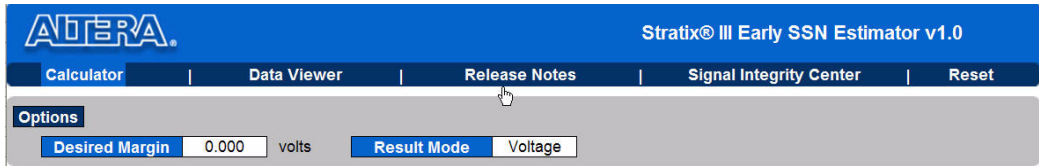
In the calculator tab, there are two kinds of parameters.

- Global parameters
- Parameters Specific to I/O Bank

Global Parameters

[Figure 1-2](#) shows the global parameters (Desired Margin and Result Mode) listed under the **Options** section in the **Calculator** tab. The ESE calculates the far-end noise, assuming a worst-case placement of pins. Worst-case pin placement assumes that aggressor pins are packed as closely as possible to the worst-case victim pin.

Figure 1–2. Defining Global Parameters



Desired Margin

The desired margin sets the amount of margin that you wish to allocate for non-SSN related items. This margin is applicable for all banks that are populated in the **Calculator** tab. By default, the ESE assumes that the entire noise margin is allocated to SSN. You can enter this in either volts or percentage of noise margin, depending on the setting you chose in Result Mode.

Result Mode

The ESE can report results using two different formats, volts and percentage margin. The default format is to report both noise and margin in volts. When in percentage margin mode, noise is still reported as volts but the margin is expressed as a percentage of the total zero-noise margin. The noise margin is calculated using the following equations:

Scenario 1

Victim Net Driven Low

$$V_{IL \text{ margin } (K)} = \left\{ 1 - \left[\frac{(QLN_{(K)} - QL)}{(VIL_{Max}(DC) - QL)} \right] \right\} * 100 \text{ where}$$

$V_{IL \text{ margin } (K)}$ = Signal Margin Low when K aggressors are switching simultaneously

K = Number of I/Os switching simultaneously

$QLN_{(K)}$ = Quiet Low Noise when K aggressors are switching simultaneously

QL = Quiet Low Voltage (No aggressors switching)

$V_{IL \text{ Max } (DC)}$ = Receiver Maximum DC Input Low Voltage

Scenario 2

Victim Net Driven High

$$V_{IH \text{ margin } (K)} = \left\{ 1 - \frac{(QH - QHN_{(K)})}{(QH - V_{IH \text{ Min}(DC)})} \right\} * 100 \text{ where}$$

$V_{IH \text{ margin } (K)}$ = Signal Margin High when K aggressors are switching simultaneously

K = Number of I/Os switching simultaneously

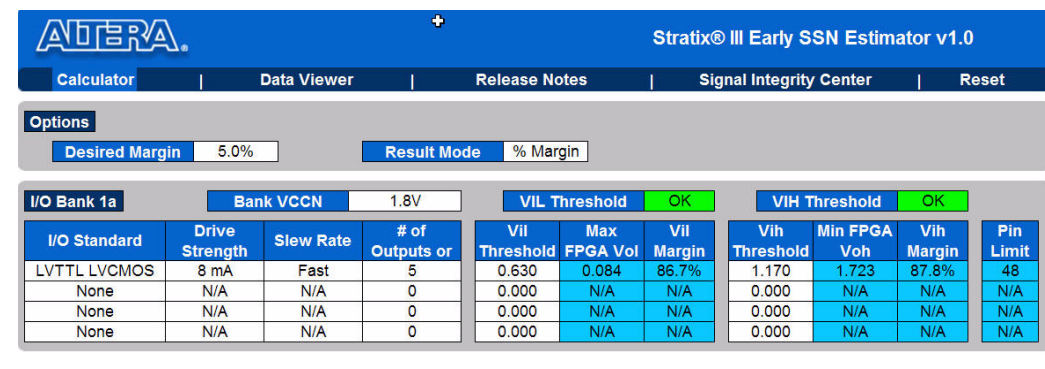
$QHN_{(K)}$ = Quiet High Noise when K aggressors are switching simultaneously

QH = Quiet High Voltage (No aggressors switching)

$V_{IH \text{ Min}(DC)}$ = Receiver Minimum DC Input High Voltage

Figure 1–3 shows the ESE estimator for Bank1a when five I/Os are switching simultaneously using LVTTTL18 8-mA drive strength with fast slew rate interface. The example in Figure 1–3 goes through the calculation to arrive at the V_{IL}/V_{IH} margin that is being reported by the ESE tool.

Figure 1–3. V_{IL}/V_{IH} Margin Calculation



From Figure 1–3 for the victim driven low, the various parameters are as follows:

$$K = 5$$

$$QLN_{(5)} = 0.084 \text{ V}$$

$$QL = 0$$

$$V_{IL \text{ max (DC)}} = 0.630 \text{ V}$$

$$V_{IL \text{ margin (5)}} = \{1 - [(0.084 - 0)/(0.63 - 0)]\} * 100 = 86.7\%$$

Similarly, for the victim driven high, the various parameters are as follows:

$$K = 5$$

$$QHN_{(5)} = 1.723 \text{ V}$$

$$QH = 1.8 \text{ V}$$

$$V_{IH \text{ min (DC)}} = 1.17 \text{ V}$$

$$V_{IH \text{ margin (5)}} = \{1 - [(1.8 - 1.723)/(1.8 - 1.17)]\} * 100 = 87.8\%$$

Parameters Specific to the I/O Bank

Figure 1–4 gives a snapshot of the ESE showing the various parameters for a given bank.

Figure 1–4. Parameters Specific to I/O Bank

ALTERA				Stratix® III Early SSN Estimator v1.0						
Calculator		Data Viewer		Release Notes		Signal Integrity Center		Reset		
Options										
Desired Margin		0.100 volts		Result Mode		Voltage				
I/O Bank 1a		Bank VCCN		VIL Threshold			VIH Threshold			
		1.8V		OK			OK			
I/O Standard	Drive Strength	Slew Rate	# of Outputs or	Vil Threshold	Max FPGA Vol	Vil Margin	Vih Threshold	Min FPGA Voh	Vih Margin	Pin Limit
HSTL Class I	8 mA	Fast	5	0.800	0.343	0.457	1.000	1.402	0.402	48
HSTL Class II	16 mA	Med-Fast	10	0.800	0.329	0.471	1.000	1.390	0.390	48
LVTTL LVCMOS	4 mA	Medium	2	0.630	0.128	0.502	1.170	1.610	0.440	48
LVTTL LVCMOS	8 mA	Slow	2	0.630	0.128	0.502	1.170	1.610	0.440	48

Bank VCCIO: All pins in an I/O bank share a common VCCIO voltage. The sharing of VCCIO voltage restricts the combinations of legal I/O standards that can be present within an I/O bank. Selecting a VCCIO voltage automatically populates the I/O standard drop-down box with the set of I/O standards that are supported by the given VCCIO voltage.

I/O Standard: The calculator supports up to four different I/O standards in a single bank. If the I/O standard you are interested in is not shown in the drop down box, ensure that the bank VCCIO voltage has been set correctly.

Drive Strength: Altera devices support multiple drive strengths depending on the I/O standard. This drop down menu allows you to select valid values.

Slew Rate: Stratix III devices support the control of output slew-rate that can be configured to balance noise and performance. A faster slew rate provides high-speed transitions for high-performance systems. A slow slew rate can help reduce system noise, but adds a nominal delay to rising and falling edges.

Number of Outputs or Bidirectional Pins: The ESE tool models simultaneously switching outputs-induced simultaneous switching noise. Switching inputs are not modeled because the ESE has no information on what device is driving an FPGA input. Enter the number of outputs or bidirectional pins that correspond to your selected I/O standard and drive strength.

$V_{IL(DC)}$ / $V_{IH(DC)}$ Thresholds: The ESE bases its margin estimates on the input thresholds of the receiving device. By default, the $V_{IL(DC)}$ and $V_{IH(DC)}$ parameters are automatically populated with their I/O standard-specific values when an I/O standard is selected. You can manually change values to any threshold values.

Not all banks shown in the ESE tool are available in all the Stratix III devices. The number of I/O banks available and bank size depends on the device density.



For more information, refer to volume 1 of the [Stratix III Device Handbook](#).

Interpreting Early SSN Estimator Results

The Stratix III ESE reports four types of results for use in guiding your early I/O design: output low/high voltages, input threshold margins, margin okay indicators, and maximum pin limit, as shown in [Figure 1–4](#).

Max FPGA V_{OL} : The maximum voltage output low parameter reports the highest voltage that an FPGA pin can output when driving a low value, taking into account SSN-induced noise.

Min FPGA V_{OH} : The minimum voltage output high parameter reports the lowest voltage that an FPGA pin can output when driving a high value, taking into account SSN-induced noise.

V_{IL} Margin/ V_{IH} Margin: This parameter indicates how much additional noise the output can tolerate before violating the $V_{IL(DC)}$ voltage input low or $V_{IH(DC)}$ voltage input high thresholds at the receiver.

V_{IL}/V_{IH} Threshold Indicator: The indicators are a quick way to verify if all the I/O standards of a given bank have sufficient margin. If all the checks pass, the indicators are green. If any margin is violated, the indicators turn red.

Pin Limit: The pin limit indicates the maximum number of pins of the corresponding I/O standard that can be used without violating noise margins, assuming that all other I/O standard pin counts are held constant. For an I/O standard, if the number of outputs switching is less than or equal to the pin limit indicated, then V_{IL}/V_{IH} threshold indicators will be green.

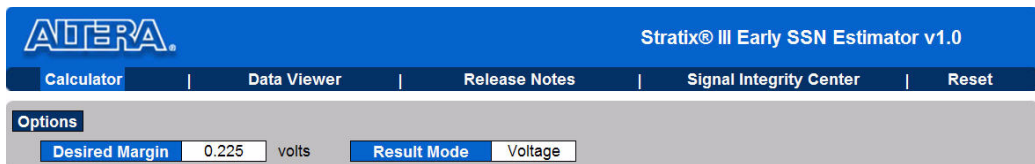
Tutorial: Mixing SSTL and LVTTTL in a Single Bank

Engineer Bob would like to add ten 1.8-V LVTTTL pins to a bank filled with ten 1.8-V SSTL Class I 12 mA and ten 1.8-V SSTL Class I 12 mA drivers. Bob is targeting a voltage margin of 225 mV to account for other non-SSN related items. Use the ESE to determine if Bob might have problems.

Step 1: Configure the Global Parameters

1. Configure Result Mode to display the results in **Voltage**.
2. Enter a desired margin of **0.225** volts, as shown in [Figure 1–5](#).

Figure 1–5. Global Parameters Configuration



Step 2: Assign I/O Standards to the Corresponding Bank

1. Set I/O Bank 1a VCCIO to 1.8 V.
2. Select I/O Standard **SSTL Class I** in row one.
3. Select a drive strength of **12 mA**.
4. Select **Fast** slew rate
5. Enter **10** as the number of output pins.
6. Select I/O Standard **SSTL Class II** in row two.
7. Select a drive strength of **16 mA**.
8. Select **Fast** slew rate.
9. Enter **10** as the number of output pins.
10. Select I/O standard **LVTTTL** in row three.
11. Select a drive strength of **12 mA**.
12. Select a **Fast** slew rate.
13. Enter **10** as the number of output pins, as shown in [Figure 1-6](#).

Figure 1-6. Local Parameters Assignment

The screenshot shows the Altera Stratix III Early SSN Estimator v1.0 interface. The 'Options' section is set to 'Desired Margin' of 0.225 volts and 'Result Mode' of Voltage. The 'I/O Bank 1a' section shows 'Bank VCCN' set to 1.8V. The 'VIL Threshold' is set to 'OK' and the 'VIH Threshold' is set to 'ERROR'. Below this, a table displays the results for three I/O standards: SSTL Class I, SSTL Class II, and LVTTTL LVCMOS. The table includes columns for I/O Standard, Drive Strength, Slew Rate, # of Outputs or, VIL Threshold, Max FPGA Vol, VIL Margin, VIH Threshold, Min FPGA Voh, VIH Margin, and Pin Limit.

I/O Standard	Drive Strength	Slew Rate	# of Outputs or	Vil Threshold	Max FPGA Vol	Vil Margin	ViH Threshold	Min FPGA Voh	ViH Margin	Pin Limit
SSTL Class I	12 mA	Fast	10	0.775	0.410	0.365	1.025	1.327	0.302	8
SSTL Class II	16 mA	Fast	10	0.775	0.435	0.340	1.025	1.247	0.222	7
LVTTTL LVCMOS	12 mA	Fast	10	0.630	0.234	0.396	1.170	1.497	0.327	8
None	N/A	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A

Step 3: Interpret the Results

- The V_{IH} threshold indicator is red indicating that a margin has been violated.
- The V_{IH} margin for SSTL Class II is 0.222 V (less than the 0.225 V that Bob wants for his design). This is highlighted in red to indicate that it is lower than the desired margin.
- The pin limit for SSTL Class II is seven pins. This means that if the number of outputs for SSTL Class II is reduced to seven, the margin will no longer be violated.
- The pin limit for LVTTL is eight pins. This means that only eight LVTTL pins can be safely combined with ten SSTL Class I and ten SSTL Class II pins under the entered drive strengths and slew rate for the given desired margin of 0.225 V set by Bob.

Step 4: Fixing the Problem

There are multiple approaches to fix the issue that Bob is observing.

First Approach

Reduce the amount of margin that Bob wishes to allocate for non-SSN-related items from 225 mV to 200 mV, as shown in [Figure 1-7](#).

The pin limit for LVTTL increased from 8 to 22, thereby allowing Bob to implement his SSTL Class I design with 10 I/Os and SSTL Class II with 10 I/Os, along with 10 LVTTL output pins.

Figure 1-7. First Approach

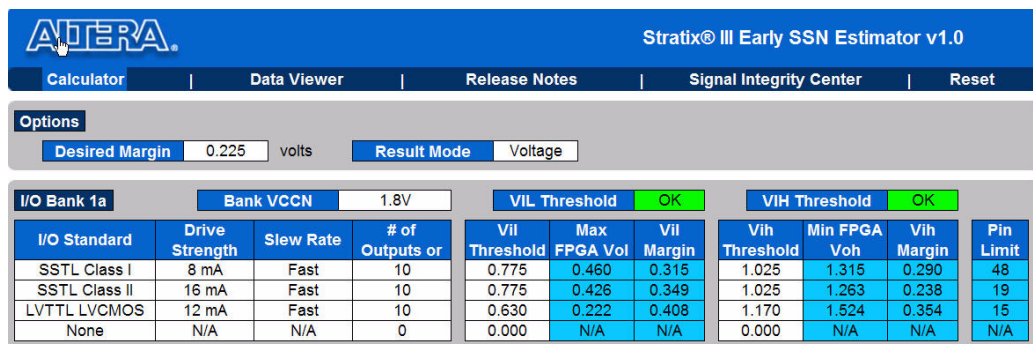
ALTERA												Stratix® III Early SSN Estimator v1.0							
Calculator			Data Viewer			Release Notes			Signal Integrity Center			Reset							
Options																			
Desired Margin			0.200 volts			Result Mod+			Voltage										
I/O Bank 1a				Bank VCCN			1.8V			VIL Threshold			OK		VIH Threshold			OK	
I/O Standard	Drive Strength	Slew Rate	# of Outputs or	Vil Threshold	Max FPGA Vol	Vil Margin	Vih Threshold	Min FPGA Voh	Vih Margin	Pin Limit									
SSTL Class I	12 mA	Fast	10	0.775	0.410	0.365	1.025	1.327	0.302	37									
SSTL Class II	16 mA	Fast	10	0.775	0.435	0.340	1.025	1.247	0.222	42									
LVTTL LVCMOS	12 mA	Fast	10	0.630	0.234	0.396	1.170	1.497	0.327	22									
None	N/A	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A									

Second Approach

If the timing margin allows, reduce the current drive strength for the SSTL Class I buffers from 12 mA to 8 mA, keeping the desired voltage margin at 225 mV for non-SSN-related items, as shown in Figure 1–8.

This decrease in drive strength reduces the SSN noise sufficiently to allow Bob to implement his design with ten SSTL Class I and ten SSTL Class II I/Os, along with ten LVTTTL I/Os with sufficient margin.

Figure 1–8. Second Approach



Third Approach

If the design allows, change the slew rate control SSTL Class II I/O to medium-fast, keeping the desired voltage margin at 225 mV for non-SSN related items, as shown in Figure 1–9.

Changing the slew rate setting from fast to medium-fast reduces the SSN noise sufficiently to allow Bob to implement his design with ten SSTL Class I and ten SSTL Class II I/Os, along with ten LVTTTL I/Os with sufficient margin.

Figure 1–9. Third Approach

ALTERA Stratix® III Early SSN Estimator v1.0

Calculator | Data Viewer | Release Notes | Signal Integrity Center | Reset

Options

Desired Margin: 0.225 volts | Result Mode: Voltage

I/O Bank 1a | Bank VCCN: 1.8V | VIL Threshold: OK | VIH Threshold: OK

I/O Standard	Drive Strength	Slew Rate	# of Outputs or	Vil Threshold	Max FPGA Vol	Vil Margin	Vih Threshold	Min FPGA Voh	Vih Margin	Pin Limit
SSTL Class I	12 mA	Med-Fast	10	0.775	0.391	0.384	1.025	1.350	0.325	48
SSTL Class II	16 mA	Fast	10	0.775	0.416	0.359	1.025	1.265	0.240	17
LVTTL LVCMOS	12 mA	Fast	10	0.630	0.208	0.422	1.170	1.529	0.359	14
None	N/A	N/A	0	0.000	N/A	N/A	0.000	N/A	N/A	N/A

