

HardCopy IV E ASIC Product Table



v0.121	HardCopy® IV E ASIC		Stratix® IV E FPGA Prototype		HardCopy IV E Resource (Stratix IV E FPGA Prototype Max Resource) ¹							
HardCopy Base Die	Package ² (Body Size)	Generic Part Number	Prototyping Device	LEs	ASIC Gates ³	I/O Pins ⁴	Full Duplex LVDS Pairs ⁵	18x18 Multipliers	PLLs	Total Embedded Memory Bits ⁶	M9Ks	M144Ks
HC4E25	WF484 (23 mm) FF484 (23 mm)	HC4E25WF484N HC4E25FF484N	EP4SE230F29 (F780) ⁷	228K	9.2 M	296 (488)	48 (56)	1288	4	10.7M (13.9M)	864 (1235)	22
			EP4SE230F29 (F780)	228K	9.2 M	392 (488)	48 (56)	1288	4	10.7M (13.9M)	864 (1235)	22
	WF780 (29 mm)	HC4E25WF780N	EP4SE360H29 (H780)	354K	9.4 M	392 (488)	48 (56)	1040	4	12.1M (17.7M)	864 (1248)	32 (48)
			EP4SE230F29 (F780)	228K	9.2 M	488	56	1288	4	10.7M (13.9M)	864 (1235)	22
	FF780 (29 mm)	HC4E25FF780N	EP4SE360H29 (H780)	354K	9.4 M	488	56	1040	4	12.1M (17.7M)	864 (1248)	32 (48)
			EP4SE230F29 (F780)	228K	9.2 M	488	56	1040	4	12.1M (17.7M)	864 (1248)	32 (48)
HC4E35	FF1152 (35 mm)	HC4E35FF1152N	EP4SE360F35 (F1152)	354K	9.4 M	744	88	1040	8	17.7M	1248	48
			EP4SE530H35 (H1152)	531K	11.5 M	744	88	1024	8	18.0M (20.3M)	1280	48 (64)
			EP4SE820H35 (H1152)	813K	14.6 M	744	88	960	8	18.4M (22.6M)	1320 (1610)	48 (60)
	FF1517 (40 mm)	HC4E35FF1517N	EP4SE530H40 (H1517)	531K	11.5 M	880 (976)	88 (112)	1024	12	18.0M (20.3M)	1280	48 (64)
			EP4SE820H40 (H1517)	813K	14.6 M	880 (976)	88 (112)	960	12	18.4M (22.6M)	1320 (1610)	48 (60)
			EP4SE530H40 (H1517)	531K	11.5 M	880 (976)	88 (112)	1024	12	18.0M (20.3M)	1280	48 (64)

1. Number outside of () indicates available resource in HardCopy device, number inside () indicates maximum resource in FPGA

2. WF: low-cost wire-bond package type; FF: performance-optimized flip-chip package type

3. Calculated as 12 gates per LE plus 5,000 gates per 18x18 multiplier. Does not include RAMs, PLLs, test circuitry, and I/O registers.

4. For the F484, F780, and F1152 packaged devices, I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) that can be used for data inputs. For the F1517 packaged devices, I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) and eight dedicated corner PLL clock inputs (PLL_L1_CLKp, PLL_L1_CLKn, PLL_L4_CLKp, PLL_L4_CLKn, PLL_R4_CLKp, PLL_R4_CLKn, PLL_R1_CLKp, and PLL_R1_CLKn) that can be used for data inputs.

5. Each full-duplex LVDS pair is comprised of one TX channel and one RX channel with DPA and soft CDR support

6. Memory bit count does not include MLAB memories which are constructed with HCells; 1 Mb = 1,024x1,024 bits

7. HardCopy devices are non-socket replacements for FPGAs