

## Introduction


The Arria™ GX device family offers up to 840-Mbps differential I/O capabilities to support source-synchronous communication protocols such as HyperTransport™ technology, Rapid I/O, XSBI, and SPI.

Arria GX devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmit serializer
- Receive deserializer
- Data realignment circuit
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog phased locked loop (PLLs) and fast PLLs

For high-speed differential interfaces, Arria GX devices can accommodate different differential I/O standards, including the following:

- LVDS
- HyperTransport technology
- HSTL
- SSTL
- LVPECL

 HSTL, SSTL, and LVPECL I/O standards can be used only for PLL clock inputs and outputs in differential mode.

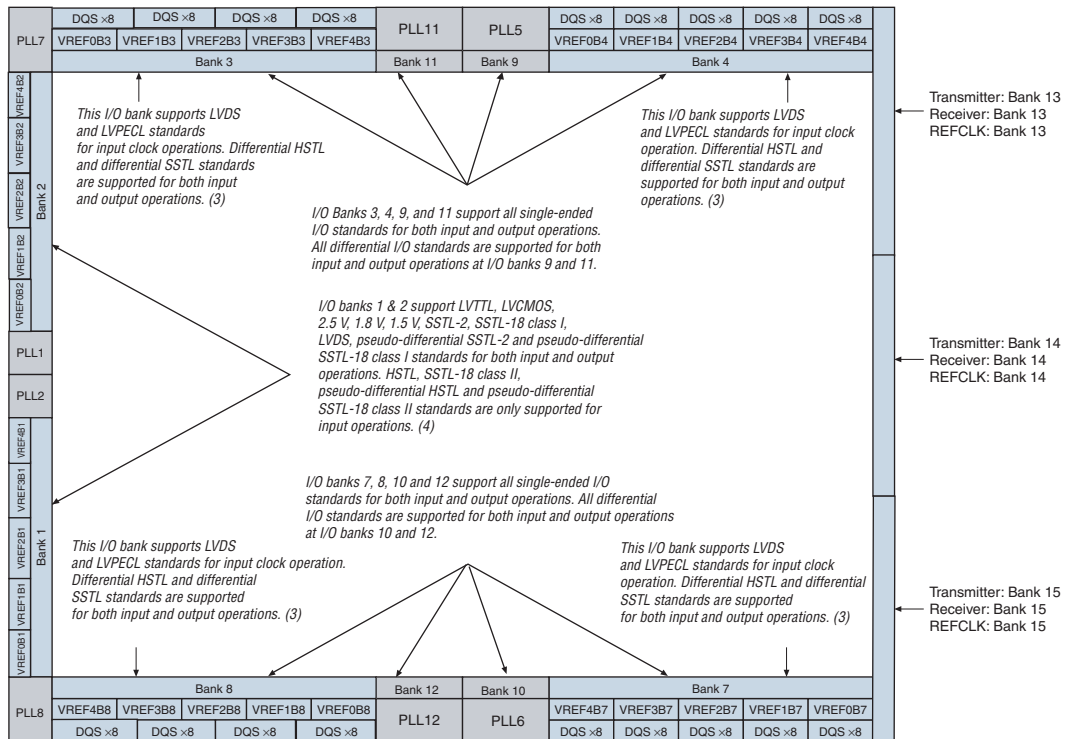
This chapter contains the following sections:

- “I/O Banks” on page 9–2
- “Differential Transmitter” on page 9–3
- “Differential Receiver” on page 9–6
- “Differential I/O Termination” on page 9–10
- “Fast PLL ” on page 9–10
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- “Differential Pin Placement Guidelines” on page 9–18
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## I/O Banks

Arria GX inputs and outputs are partitioned into banks located on the periphery of the die. The inputs and outputs that support LVDS and HyperTransport technology are located in row I/O banks, on the left side of the Arria GX device. LVPECL, HSTL, and SSTL standards are supported on certain top and bottom banks of the die (banks 9 to 12) when used as differential clock inputs/outputs. Differential HSTL and SSTL standards can be supported on banks 3, 4, 7, and 8 if the pins on these banks are used as DQS pins. Figure 9–1 shows where the banks and the PLLs are located on the die.

Figure 9–1. Arria GX I/O Banks Notes (1), (2), (3), (4), (5), and (6)



### Notes to Figure 9–1:

- Figure 9–1 is a top view of the silicon die which corresponds to a reverse view for flip-chip packages. It is a graphical representation only.
- Depending on size of the device, different device members have different numbers of  $V_{REF}$  groups. Refer to the pin list and the Quartus® II software for exact locations.
- Banks 9 through 12 are enhanced PLL external clock output banks.
- Horizontal I/O banks feature transceiver and dynamic phase alignment (DPA) circuitry for high speed differential I/O standards.
- Quartus II software does not support differential SSTL and differential HSTL standards at left/right I/O banks.
- Number of available PLLs and corresponding I/O banks vary with package options.

Table 9–1 shows the total number of differential channels available in Arria GX devices. Non-dedicated clocks in the left bank can also be used as data receiver channels. The total number of receiver channels includes these four non-dedicated clock channels. Pin migration is available for different size devices in the same package.

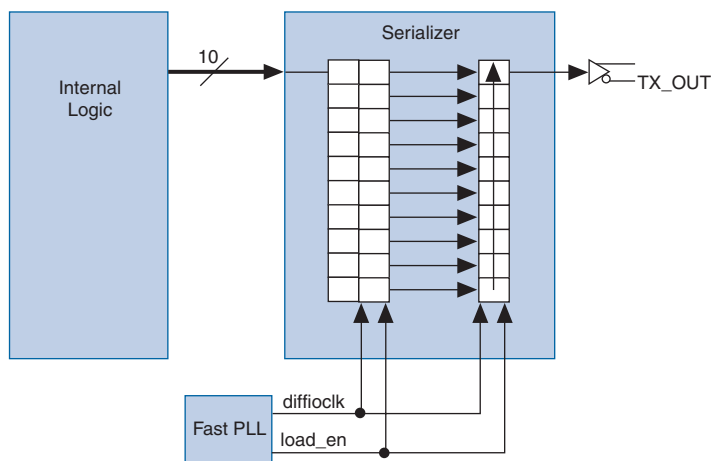
Device	484-Pin FineLine BGA	780-Pin FineLine BGA	1,152-Pin FineLine BGA
EP1AGX20	29 transmitters 31 receivers	29 transmitters 31 receivers	—
EP1AGX35	29 transmitters 31 receivers	29 transmitters 31 receivers	—
EP1AGX50	29 transmitters 31 receivers	29 transmitters 31 receivers	42 transmitters 42 receivers
EP1AGX60	29 transmitters 31 receivers	29 transmitters 31 receivers	42 transmitters 42 receivers
EP1AGX90	—	—	47 transmitters 47 receivers

**Notes to Table 9–1:**

- (1) Pin count does not include dedicated PLL input pins.
- (2) The total number of receiver channels includes the four non-dedicated clock channels that can optionally be used as data channels.

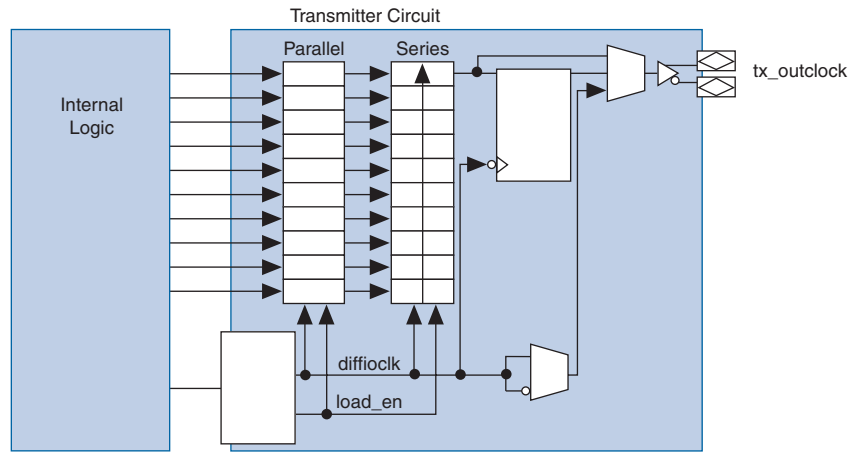
## Differential Transmitter

The Arria GX transmitter has dedicated circuitry to provide support for LVDS and HyperTransport signaling. The dedicated circuitry consists of a differential buffer, a serializer, and a shared fast PLL. The differential buffer can drive out LVDS or HyperTransport signal levels that are statically set in the Quartus II software. The serializer takes data from a parallel bus up to 10-bits wide from the internal logic, clocks it into the load registers, and serializes it using the shift registers before sending the data to the differential buffer. The most significant bit (MSB) is transmitted first. The load and shift registers are clocked by the `diffioclk` (a fast PLL clock running at the serial rate) and controlled by the load enable signal generated from the fast PLL. The serialization factor can be statically set to  $\times 4$ ,  $\times 5$ ,  $\times 6$ ,  $\times 7$ ,  $\times 8$ ,  $\times 9$  or  $\times 10$  using the Quartus II software. The load enable signal is automatically generated by the fast PLL and is derived from the serialization factor setting. Figure 9–2 is a block diagram of the Arria GX transmitter.

**Figure 9–2. Transmitter Block Diagram**

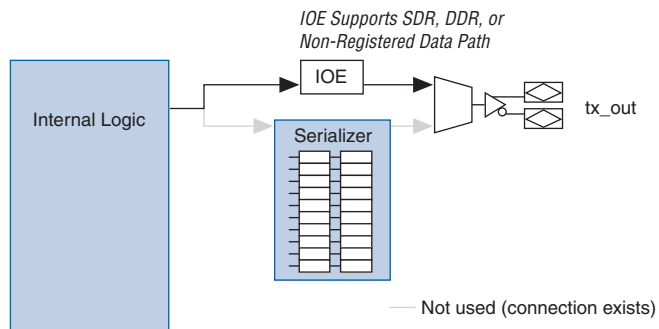
Each Arria GX transmitter data channel can be configured to operate as a transmitter clock output. This flexibility allows the designer to place the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. Different applications often require specific clock-to-data alignments or specific data-rate to clock-rate factors. The transmitter can output a clock signal at the same rate as the data with a maximum frequency of 717 MHz. The output clock can also be divided by a factor of 2, 4, 8, or 10, depending on the serialization factor. The phase of the clock in relation to the data can be set at  $0^\circ$  or  $180^\circ$  (edge or center aligned). The fast PLL provides additional support for other phase shifts in  $45^\circ$  increments. These settings are made statically in the Quartus II MegaWizard<sup>®</sup> software. [Figure 9–3](#) shows the transmitter in clock output mode.

**Figure 9–3. Transmitter in Clock Output Mode**



The serializer can be bypassed to support DDR ( $\times 2$ ) and SDR ( $\times 1$ ) operations. The I/O element (IOE) contains two data output registers that each can operate in either DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the fast PLL, or from the enhanced PLL. Figure 9–4 shows the bypass path.

**Figure 9–4. Serializer Bypass**



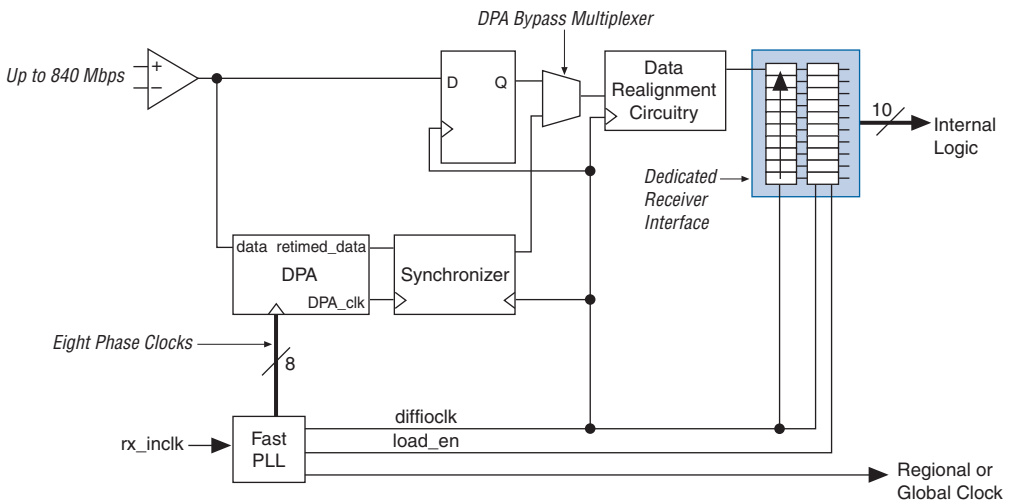
## Differential Receiver

The receiver has dedicated circuitry to support high-speed LVDS and HyperTransport signaling, along with enhanced data reception. Each receiver consists of a differential buffer, dynamic phase aligner (DPA), synchronization FIFO buffer, data realignment circuit, deserializer, and a shared fast PLL. The differential buffer receives LVDS or HyperTransport signal levels, which are statically set by the Quartus II software. The DPA block aligns the incoming data to one of eight clock phases to maximize the receiver's skew margin. The DPA circuit can be bypassed on a channel-by-channel basis if it is not needed. Set the DPA bypass statically in the Quartus II MegaWizard Plug-In Manager or dynamically by using the optional `RX_DPLL_ENABLE` port.

The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA block and the deserializer. If necessary, the data realignment circuit inserts a single bit of latency in the serial bitstream to align the word boundary. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic. The data path in the receiver is clocked by either the `diffiocl` signal or the DPA recovered clock. The deserialization factor can be statically set to 4, 5, 6, 7, 8, 9, or 10 by using the Quartus II software. The fast PLL automatically generates the load enable signal, which is derived from the deserialization factor setting.

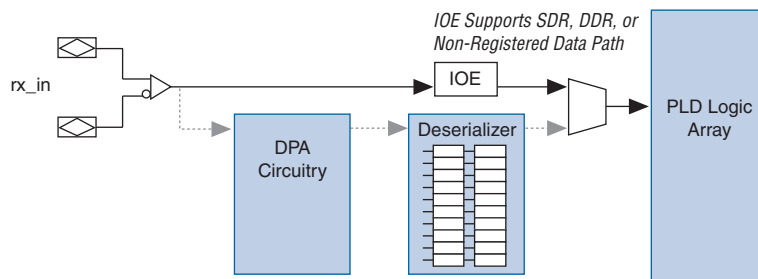
Figure 9–5 shows a block diagram of the receiver.

**Figure 9–5. Receiver Block Diagram**



The deserializer, like the serializer, can also be bypassed to support DDR ( $\times 2$ ) and SDR ( $\times 1$ ) operations. The DPA and data realignment circuit cannot be used when the deserializer is bypassed. The IOE contains two data input registers that can operate in DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the fast PLL, or from the enhanced PLL. Figure 9–6 shows the bypass path.

**Figure 9–6. Deserializer Bypass**



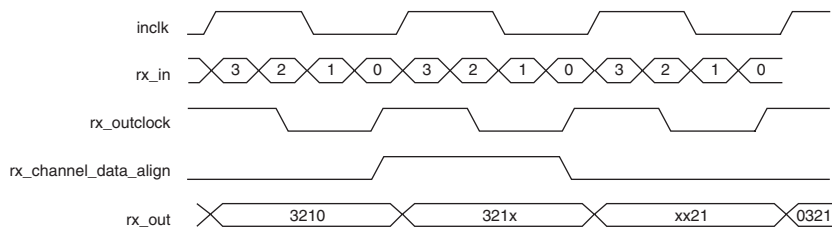
## Receiver Data Realignment Circuit

The data realignment circuit aligns the word boundary of the incoming data by inserting bit latencies into the serial stream. An optional `RX_CHANNEL_DATA_ALIGN` port controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit for every pulse on the `RX_CHANNEL_DATA_ALIGN` port. The following are requirements for the `RX_CHANNEL_DATA_ALIGN` port:

- The minimum pulse width is one period of the parallel clock in the logic array.
- The minimum low time between pulses is one period of parallel clock.
- There is no maximum high or low time.
- Valid data is available two parallel clock cycles after the rising edge of `RX_CHANNEL_DATA_ALIGN`.

Figure 9–7 shows receiver output (RX\_OUT) after one bit slip pulse with the deserialization factor set to 4.

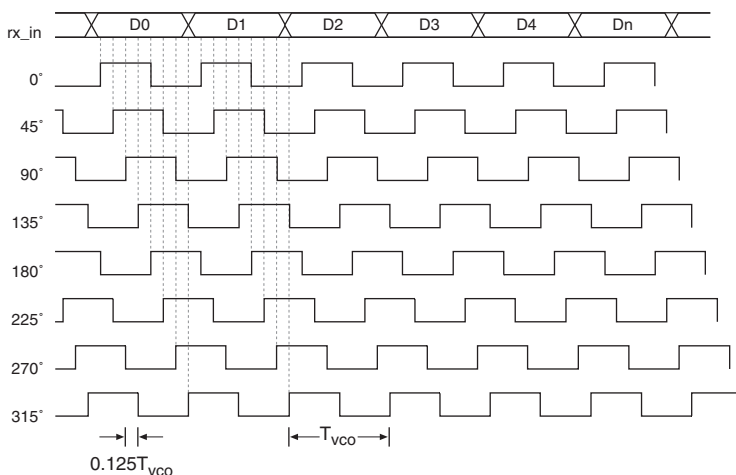
**Figure 9–7. Data Realignment Timing**



The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. The programmable bit rollover point can be from 1 to 11 bit-times independent of the deserialization factor. An optional status port, RX\_CDA\_MAX, is available to the FPGA from each channel to indicate when the preset rollover point is reached.

## Dynamic Phase Aligner

The DPA block takes in high-speed serial data from the differential input buffer and selects one of eight phase clocks to sample the data. The DPA chooses a phase closest to the phase of the serial data. The maximum phase offset between the data and the phase-aligned clock is  $1/8$  UI, which is the maximum quantization error of the DPA. The eight phases are equally divided, giving a  $45^\circ$  resolution. Figure 9–8 shows the possible phase relationships between the DPA clocks and the incoming serial data.

**Figure 9–8. DPA Clock Phase to Data Bit Relationship**

Each DPA block continuously monitors the phase of the incoming data stream and selects a new clock phase if needed. The selection of a new clock phase can be prevented by the optional `RX_DPLL_HOLD` port, which is available for each channel.

The DPA block requires a training pattern and a training sequence of at least 256 repetitions of the training pattern. The training pattern is not fixed, so you can use any training pattern with at least one transition on each channel. An optional output port, `RX_DPA_LOCKED`, is available to the internal logic, to indicate when the DPA block has settled on the closest phase to the incoming data phase. The `RX_DPA_LOCKED` de-asserts, depending on what is selected in the Quartus II MegaWizard Plug-In, when either a new phase is selected, or when the DPA has moved two phases in the same direction. The data may still be valid even when the `RX_DPA_LOCKED` is deasserted. Use data checkers to validate the data when `RX_DPA_LOCKED` is deasserted.

An independent reset port, `RX_RESET`, is available to reset the DPA circuitry. The DPA circuit must be retrained after reset.

### Synchronizer

The synchronizer is a 1-bit  $\times$  6-bit deep FIFO buffer that compensates for the phase difference between the recovered clock from the DPA circuit and the `diffioclk` that clocks the rest of the logic in the receiver. The synchronizer can only compensate for phase differences, not frequency differences between the data and the receiver's `INCLK`. An optional port,

`RX_FIFO_RESET`, is available to the internal logic to reset the synchronizer. The synchronizer is automatically reset when the DPA first locks to the incoming data. Altera® recommends using `RX_FIFO_RESET` to reset the synchronizer when the DPA signals a loss-of-lock condition beyond the initial locking condition.

## Differential I/O Termination

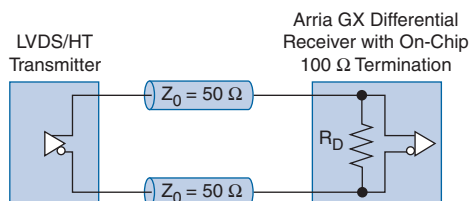
Arria GX devices provide an on-chip 100- $\Omega$  differential termination option on each differential receiver channel for LVDS and HyperTransport standards. The on-chip termination (OCT) eliminates the need to supply an external termination resistor, simplifying the board design and reducing reflections caused by stubs between the buffer and the termination resistor. You can enable on-chip termination in the Quartus II assignments editor. Differential on-chip termination is supported across the full range of supported differential data rates.



For more information regarding differential on-chip termination, refer to the High-Speed I/O Specifications section of the *DC & Switching Characteristics* chapter in volume 1 of the *Arria GX Device Handbook*.

Figure 9–9 illustrates on-chip termination.

**Figure 9–9. On-Chip Differential Termination**



On-chip differential termination is supported on all row I/O pins and on clock pins `CLK[0, 2, 8, 10]`. The clock pins `CLK[1, 3, 9, 11]`, and `FPLL[7..10]CLK`, and the clocks in the top and bottom I/O banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

## Fast PLL

The high-speed differential I/O receiver and transmitter channels use fast PLL to generate the parallel global clocks (`rx-` or `tx-` clock) and high-speed clocks (`diffioclk`). Figure 9–10 shows the locations of the fast PLLs. The fast PLL VCO operates at the clock frequency of the data rate. Each fast PLL offers a single serial data rate support, but up to two separate serialization and/or deserialization factors (from the `C0` and `C1`

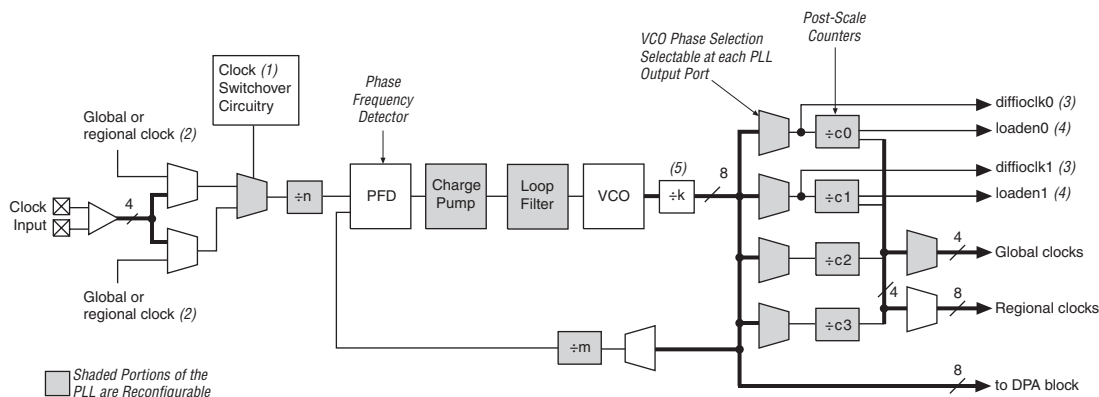
fast PLL clock outputs) can be used. Clock switchover and dynamic fast PLL reconfiguration is available in high-speed differential I/O support mode.



For additional information about the fast PLL, refer to the *PLLs in Arria GX Devices* chapter in volume 2 of the *Arria GX Handbook*.

Figure 9–10 shows a block diagram of the fast PLL in high-speed differential I/O support mode.

**Figure 9–10. Fast PLL Block Diagram**



**Notes to Figure 9–10:**

- (1) Arria GX fast PLLs only support manual clock switchover.
- (2) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or pin-driven dedicated global or regional clock.
- (3) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Arria GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.
- (4) This signal is a high-speed differential I/O support SERDES control signal.
- (5) If the design enables this  $\div 2$  counter, the device can use a VCO frequency range of 150 to 520 MHz.

## Clocking

The fast PLLs feed in to the differential receiver and transmitter channels through the LVDS/DPA clock network. The center fast PLLs can independently feed the banks above and below them. The corner PLLs can feed only the banks adjacent to them.

Figures 9-11 and 9-12 show the Fast PLL and LVDS/DPA clock of the Arria GX devices.

**Figure 9-11. Fast PLL and LVDS/DPA Clock for EP1AGX20C, EP1AGX35C/D, EP1AGX50C/D, and EP1AGX60C/D Devices**

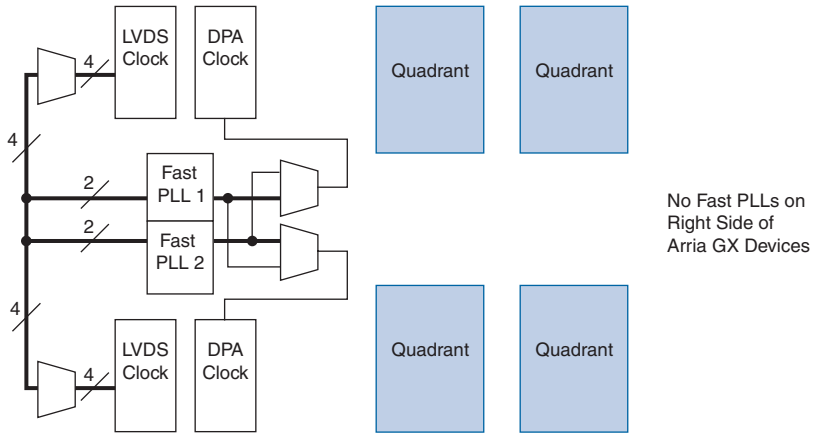
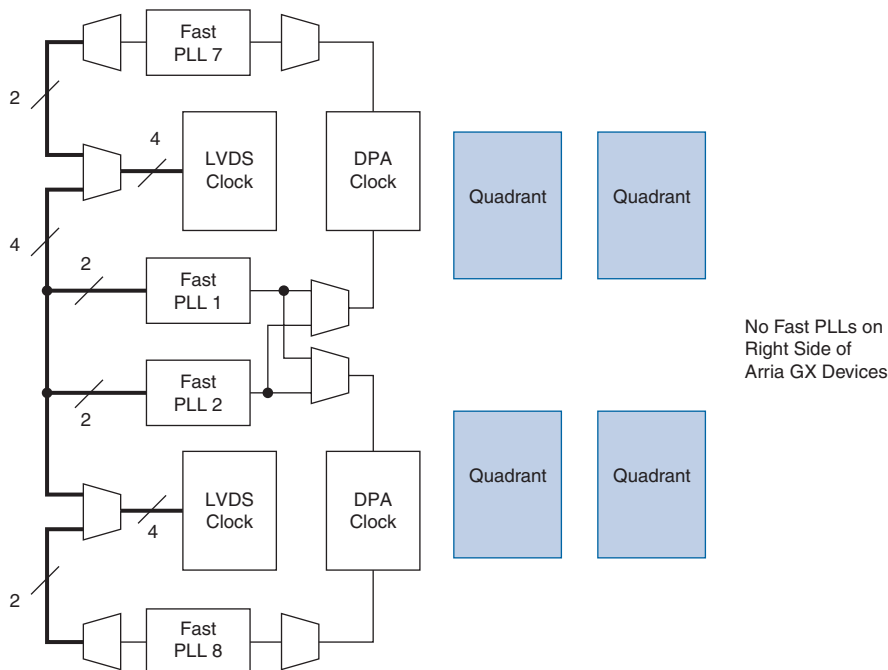


Figure 9–12. Fast PLL and LVDS/DPA Clocks for EP1AGX60E and EP1AGX90E Devices



## Source Synchronous Timing Budget

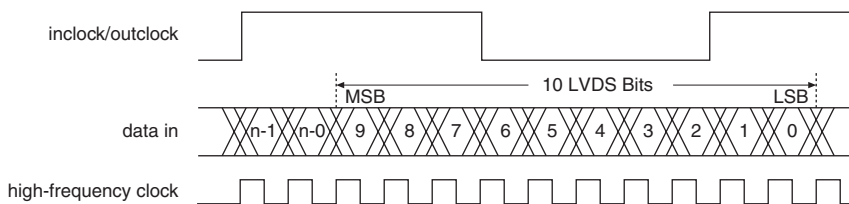
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Arria GX devices. LVDS and HyperTransport I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source-synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Arria GX devices, and how to use these timing parameters to determine a design's maximum performance.

## Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For operation at 840 Mbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. [Figure 9–13](#) shows the data bit orientation of the  $\times 10$  mode.

**Figure 9–13. Bit Orientation in the Quartus II Software**



## Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. [Figure 9–14](#) shows the data bit orientation for a channel operation. These figures are based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors use the Quartus II software tools and find the bit position within the word. The bit positions after deserialization are listed in [Table 9–2](#).

Figure 9–14 also shows a functional waveform. Timing waveforms may produce different results. Altera recommends performing a timing simulation to predict actual device behavior.

**Figure 9–14. Bit Order for One Channel of Differential Data**

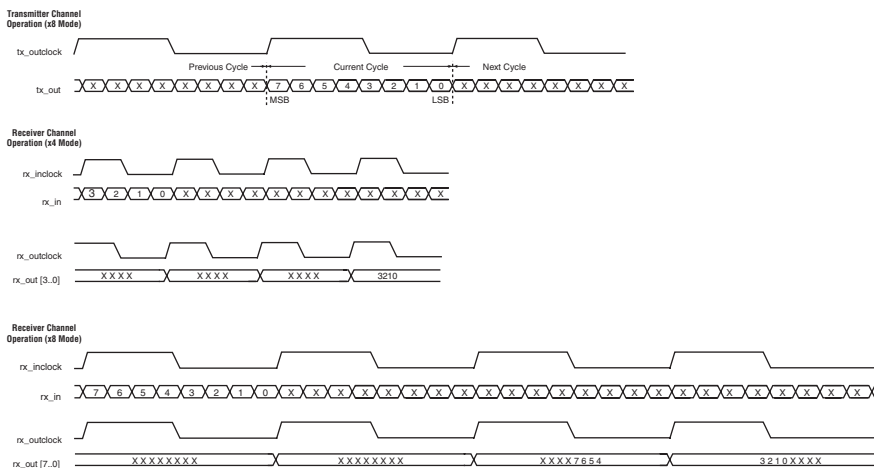


Table 9–2 shows the conventions for differential bit naming for 18 differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56
9	71	64
10	79	72
11	87	80

**Table 9–2. LVDS Bit Naming (Part 2 of 2)**

Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
12	95	88
13	103	96
14	111	104
15	119	112
16	127	120
17	135	128
18	143	136

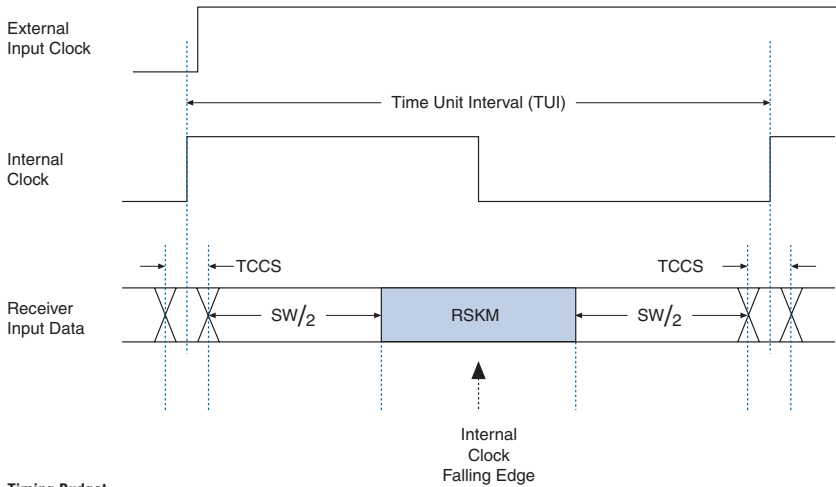
### Receiver Skew Margin for Non-DPA

Changes in system environment, such as temperature, media (cable, connector, or PCB) loading effect, the receiver's setup and hold times, and internal skew, reduce the sampling window for the receiver. The timing margin between the receiver's clock input and the data input sampling window is called Receiver Skew Margin (RSKM). [Figure 9–15](#) shows the relationship between the RSKM and the receiver's sampling window.

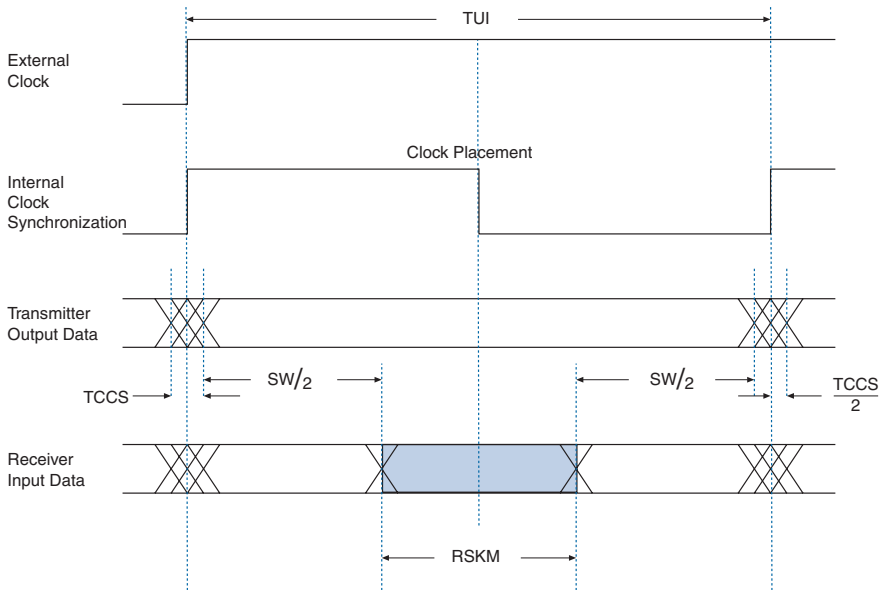
TCCS, RSKM, and the sampling window specifications are used for high-speed source-synchronous differential signals without DPA. When using DPA, these specifications are exchanged for the simpler single DPA jitter tolerance specification. For instance, the receiver skew is why each input with DPA selects a different phase of the clock, thus removing the requirement for this margin.

**Figure 9–15. Differential High-Speed Timing Diagram and Timing Budget for Non-DPA**

Timing Diagram



Timing Budget



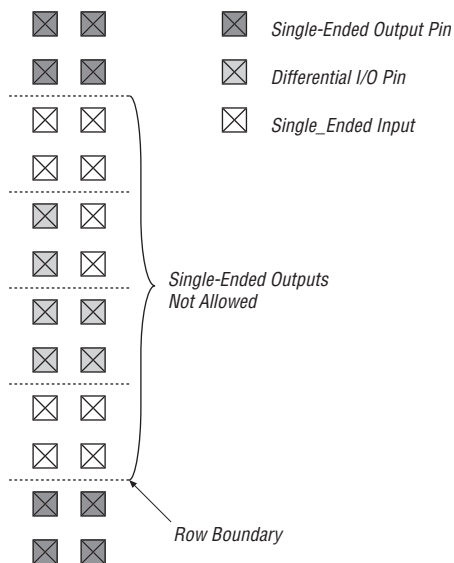
## Differential Pin Placement Guidelines

In order to ensure proper high-speed operation, differential pin placement guidelines have been established. The Quartus II compiler automatically checks that these guidelines are followed and will issue an error message if these guidelines are not met. PLL driving distance information is separated into guidelines with and without DPA usage.

### High-Speed Differential I/Os and Single-Ended I/Os

When a differential channel or channels of side banks are used (with or without DPA), you must adhere to the guidelines described in the following sections.

- Single-ended I/Os are allowed in the same bank as the LVDS channels (with or without DPA) as long as the single-ended I/O standard uses the same  $V_{CCIO}$  as the LVDS bank.
- Single-ended inputs can be in the same logic array block (LAB) row. Outputs cannot be on the same LAB row with LVDS I/Os. If input registers are used in the I/O cell (IOC), single-ended inputs cannot be in the same LAB row as an LVDS SERDES block.
- LVDS (non-SERDES) I/Os are allowed in the same row as LVDS SERDES but the use of IOC registers are not allowed.
- Single-ended outputs are limited to 120 mA drive strength on LVDS banks (with or without DPA).
  - LVTTL equation for maximum number of I/Os in an LVDS bank:
    - $120 \text{ mA} = (\text{number of LVTTL outputs}) \times (\text{drive strength of each LVTTL output})$
  - SSTL-2 equation:
    - $120 \text{ mA} = (\text{number of SSTL-2 I/Os}) \times (\text{drive strength of each output}) \div 2$
  - LVTTL and SSTL-2 mix equation:
    - $120 \text{ mA} = (\text{total drive strength of all LVTTL outputs}) + (\text{total drive strength of all SSTL2 outputs}) \div 2$
- Single-ended inputs can be in the same LAB row as a differential channel using the SERDES circuitry; however, IOE input registers are not available for the single-ended I/Os placed in the same LAB row as differential I/Os. The same rule for input registers applies for non-SERDES differential inputs placed within the same LAB row as a SERDES differential channel. The input register must be implemented within the core logic. The same rule for input registers applies for non-SERDES differential inputs placed within the same LAB row as a SERDES differential channel.
- Single-ended output pins must be at least one LAB row away from differential output pins, as shown in [Figure 9–16](#).

**Figure 9–16. Single-Ended Output Pin Placement with Respect to Differential I/O Pins**

## DPA Usage Guidelines

Arria GX devices have differential receivers and transmitters on the Row banks of the device. Each receiver has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel. When a channel or channels are used in DPA mode, the guidelines listed below must be adhered to.

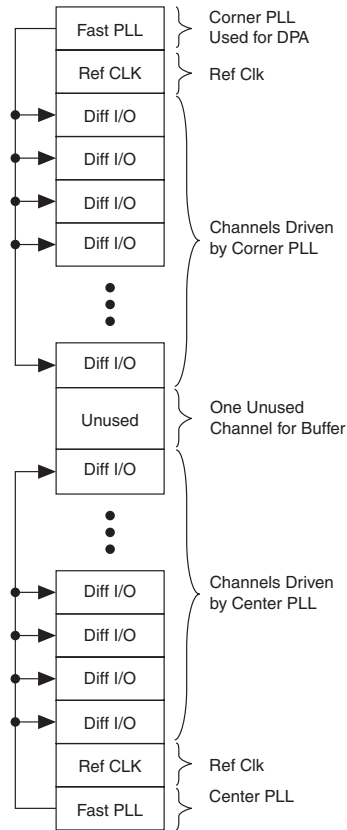
### *Fast PLL/DPA Channel Driving Distance*

- If the number of DPA channels driven by each center or corner fast PLL exceeds 25 LAB rows, Altera recommends you implement data realignment (bit-slip) circuitry for all the DPA channels.
- If one center fast PLL drives DPA channels in the upper and lower banks, the other center fast PLL cannot be used for DPA.

*Using Corner and Center Fast PLLs*

- If a differential bank is being driven by two fast PLLs, where the corner PLL is driving one group and the center fast PLL is driving another group, there must be at least one row of separation between the two groups of DPA channels (see [Figure 9-17](#)). The two groups can operate at independent frequencies. Not all the channels are bonded out of the die. Each LAB row is considered a channel, whether or not it has I/O support.
- No separation is necessary if a single fast PLL is driving DPA channels as well as non-DPA channels as long as the DPA channels are contiguous.

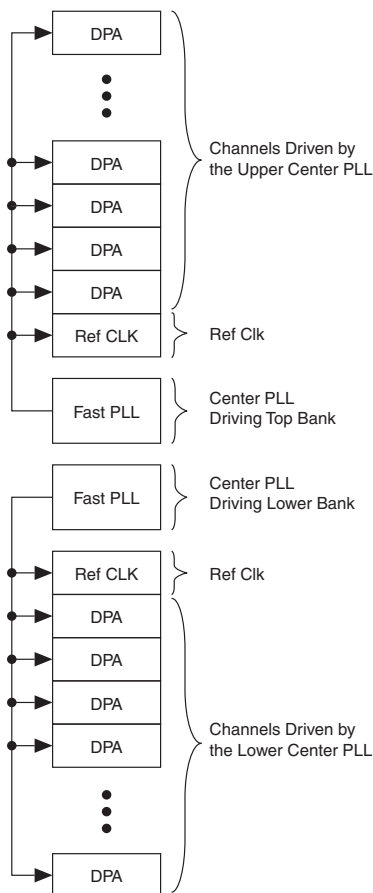
**Figure 9-17. Usage of Corner and Center Fast PLLs Driving DPA Channels in a Single Bank**



*Using Both Center Fast PLLs*

- Both center fast PLLs can be used for DPA as long as they drive DPA channels in their adjacent quadrant only (see [Figure 9–18](#)).
- Both center fast PLLs cannot be used for DPA if one of the fast PLLs drives the top and bottom banks, or if they are driving cross banks (for example, the lower fast PLL drives the top bank and the top fast PLL drives the lower bank).

**Figure 9–18. Center Fast PLL Usage When Driving DPA Channels**



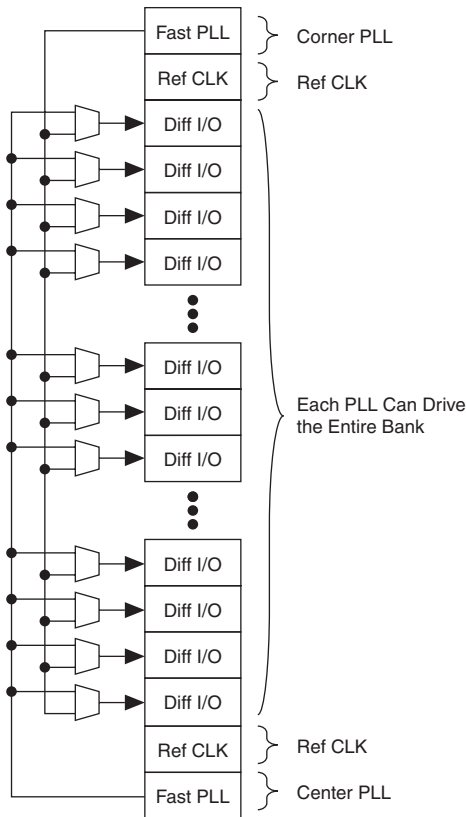
## Non-DPA Differential I/O Usage Guidelines

When a differential channel or channels of left or right banks are used in non-DPA mode, you must adhere to the guidelines in the following sections.

### Fast PLL/Differential I/O Driving Distance

- Each fast PLL can drive all the channels in the entire bank, as shown in Figure 9-19.

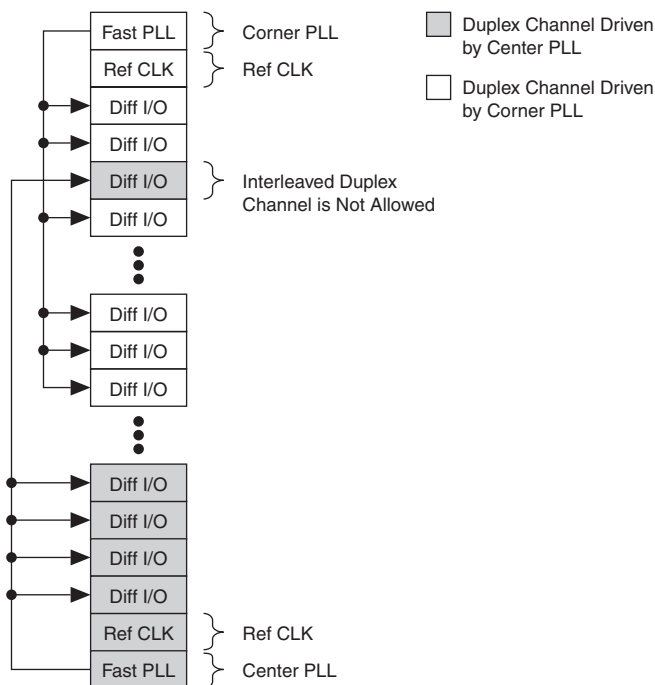
**Figure 9-19. Fast PLL Driving Capability When Driving Non-DPA Differential Channels**



### Using Corner and Center Fast PLLs

- The corner and center fast PLLs can be used as long as the channels driven by separate fast PLLs do not have their transmitter or receiver channels interleaved. [Figure 9–20](#) shows illegal placement of differential channels when using corner and center fast PLLs.
- If one fast PLL is driving transmitter channels only, and the other fast PLL drives receiver channels only, the channels driven by those fast PLLs can overlap each other.
- Center fast PLLs can be used for both transmitter and receiver channels.

**Figure 9–20. Illegal Placement of Interlaced Duplex Channels in an I/O Bank**



## Board Design Considerations



This section explains how to achieve the optimal performance from the Arria GX high-speed I/O block and ensure first-time success in implementing a functional design with optimal signal quality.

For more information about board layout recommendations and I/O pin terminations, refer to [AN 224: High-Speed Board Layout Guidelines](#).

To achieve the best performance from the device, pay attention to the impedances of traces and connectors, differential routing, and termination techniques.

The Arria GX high-speed module generates signals that travel over the media at frequencies as high as 840 Mbps. Board designers should use the following guidelines:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.
- Place external reference resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° or 45° corners.
- Use high-performance connectors such as HMZD or VHDM connectors for backplane designs. Two suppliers of high-performance connectors are Teradyne Corp ([www.teradyne.com](http://www.teradyne.com)) and Tyco International Ltd. ([www.tyco.com](http://www.tyco.com)).
- Design backplane and card traces so that trace impedance matches the connector's or the termination's impedance.
- Keep an equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths also result in misplaced crossing points and system margins when the transmitter-channel-to-channel skew (TCCS) value increases.
- Limit vias, because they cause impedance discontinuities.
- Use the common bypass capacitor values such as 0.001, 0.01, and 0.1  $\mu\text{F}$  to decouple the fast PLL power and ground planes. You can also use 0.0047  $\mu\text{F}$  and 0.047  $\mu\text{F}$ .
- Keep switching TTL signals away from differential signals to avoid possible noise coupling.
- Do not route transistor-to-transistor logic (TTL) clock signals to areas under or above the differential signals.
- Route signals on adjacent layers orthogonally to each other.

## Conclusion

Arria GX high-speed differential inputs and outputs, with their DPA and data realignment circuitry, allow users to build a robust multi-Gigabit system. The DPA circuitry allows users to compensate for any timing skews resulting from physical layouts. The data realignment circuitry allows the devices to align the data packet between the transmitter and receiver. Together with the on-chip differential termination, Arria GX devices can be used as a single-chip solution for high-speed applications.

## Referenced Documents

This chapter references the following documents:

- *AN 224: High-Speed Board Layout Guidelines*
- *DC & Switching Characteristics* chapter in volume 1 of the *Arria GX Device Handbook*
- *PLLs in Arria GX Devices* chapter in volume 2 of the *Arria GX Handbook*

## Document Revision History

Table 9–3 shows the revision history for this chapter.

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
May 2008 v1.2	Updated: <ul style="list-style-type: none"> <li>● “DPA Usage Guidelines”</li> <li>● “Fast PLL/DPA Channel Driving Distance”</li> </ul>	—
	Updated Figure 9–15.	—
	Minor text edits.	—
August 2007 v1.1	Added the “Referenced Documents” section.	—
	Minor text edits.	—
May 2007 v1.0	Initial release.	—

